REMARKS

The Office Action dated March 9, 2005, has been received and carefully considered. In this response, claims 49, 61, 77, 80-82, 86-88, and 90-93 have been amended. Entry of the amendments to claims 49, 61, 77, 80-82, 86-88, and 90-93 is respectfully requested. Reconsideration of the outstanding objections/rejections in the present application is also respectfully requested based on the following remarks.

At the outset, Applicants note with appreciation the indication on page 4 of the Office Action that claims 54, 55, 66, 67, and 79 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicants have opted to defer rewriting the above-identified claims in independent form pending reconsideration of the arguments presented below with respect to the rejected independent claims.

I. THE OBJECTION TO CLAIMS 90-93

Claims 90-93 were objected to for lacking a positive limitation.

The Examiner asserts that the term "adapted to" is not a positive limitation.

While Applicants disagree with the Examiner's assertion, claims 90-93 have been amended to address the Examiner's concerns.

In view of the foregoing, it is respectfully requested that the aforementioned objection to claims 90-93 be withdrawn.

II. THE ENABLEMENT REJECTION OF CLAIMS 90 and 92

Claims 90 and 92 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. This rejection is hereby respectfully traversed.

The Examiner asserts that the specification does not support receiving parallel data in a transmit circuit and outputting parallel data in a receive circuit.

Applicants disagree. Support for such limitations are found throughout the specification, but specifically, for example, at page 11, lines 20-23; page 16, lines 26-28; page 38, lines 24-27; page 39, lines 10-13; etc. (i.e., paragraphs [45], [61], [134], [137], etc. in U.S. Patent Application Publication No. US2003/0208707A9).

In view of the foregoing, it is respectfully requested that the aforementioned enablement rejection of claims 90 and 92 be withdrawn.

III. THE ANTICIPATION REJECTION OF CLAIMS 77, 78, AND 80-88

Claims 77, 78, and 80-88 were rejected under 35 U.S.C. § 102(e) as being anticipated by Johnson et al. (U.S. Patent No. 6,606,041). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id.. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's

description of the invention with his own knowledge to make the claimed invention." Id..

Regarding claim 77, the Examiner asserts that Johnson et al. teaches a method for operating a transmit circuit as claimed. Specifically, the Examiner asserts that Johnson et al. teaches passing data through the transmit end (FIG. 2, DQ to 51 to 59 to 63 to SRAM) in a normal operating mode, and to provide for evaluation of a digital signal (column 12, lines 5-13 and circuit of FIG. 6) by generating a repeating pattern (FIG. 6 connected to DQ) when in test mode.

However, it is respectfully submitted that the Examiner has failed to address several recited features of claim 77. For instance, claim 77 recites passing transmit data through the transmit circuit when the transmit circuit is operating in a normal mode. It is respectfully submitted that Johnson et al. does not teach that transmit data is passed through a transmit circuit. Indeed, Figure 2 of Johnson et al., and the path from DQ to 51 to 59 to 63 to 67 to 71 in Figure 2 in particular, shows data being received at an SLDRAM module 11 (see column 4, lines 15-53). The data is in fact transmitted from a memory controller 13 and received by the SLDRAM module 11 (see column 4, lines 54-61). Thus, Applicants respectfully request that the Examiner specifically address what elements of Johnson et al.,

if any, perform the claimed function of passing transmit data through the transmit circuit when the transmit circuit is operating in a normal mode, as claimed.

Claim 77 also recites generating a transmit repeating pattern in the transmit circuit when the transmit circuit is operating in a test mode. It is respectfully submitted that Johnson et al. does not teach that a transmit repeating pattern is generated in the SLDRAM module 11. Indeed, the Examiner acknowledges this by asserting that a synchronizing pattern may be generated in the circuit of Figure 6, which is located in the memory controller 13 (see column 5, lines 57-59, and column 9, lines 34-54). Obviously, the SLDRAM module 11 and the memory controller 13 and separate and distinct circuits, with one being a transmitter and the other being a receiver. It is respectfully submitted that it is improper to selectively pick and chose separate and distinct portions of Johnson et al. based on hindsight in view of claim 77. Thus, Applicants respectfully request that the Examiner specifically address what elements of Johnson et al., if any, perform the claimed function of generating a transmit repeating pattern in the transmit circuit when the transmit circuit is operating in a test mode, as claimed.

Lastly, claim 77 is directed toward a method for operating a transmit circuit to provide for evaluation of a digital signaling system. In contrast, Johnson et al. is directed (as acknowledged by the Examiner) toward a method of calibrating a data path. It is respectfully submitted that evaluating is different than calibrating, as the former does not necessarily include the latter.

At this point it should be noted that claim 77 has been amended solely for purposes of clarity and to insure that there is proper antecedent basis throughout the claims.

In view of the foregoing, it is respectfully submitted that claim 77 is not anticipated by Johnson et al..

Claims 78 and 80-82 are dependent upon independent claim 77. Thus, since independent claim 77 should be allowable as discussed above, claims 78 and 80-82 should also be allowable at least by virtue of their dependency on independent claim 77. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 78 recites that the step of generating a transmit repeating pattern in the transmit circuit further comprises the step of preloading an initialization pattern into the transmit circuit. It is respectfully submitted that Johnson et al. fails to claim,

disclose, or even suggest such a feature. Also, claim 80 recites that the step of passing transmit data through the transmit circuit further comprises the step of passing distinct data through each of the plurality of pipeline structures when the transmit circuit is operating in the normal mode. As previously discussed in the Amendment/Response filed May 17, 2004, it is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature. Further, claim 81 recites that the method further comprises the steps of receiving the transmit data in a receive circuit when the transmit circuit is operating in the normal mode, and receiving the transmit repeating pattern in the receive circuit when the transmit circuit is operating in the test mode. It is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature. Additionally, claim 82 recites that the method further comprises the steps of receiving the transmit data in a receive circuit when the transmit circuit is operating in the normal mode, and receiving the transmit repeating pattern in a test receiver separate from the receive circuit when the transmit circuit is operating in the test mode. It is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature.

At this point it should be noted that claims 80-82 have been amended solely for purposes of clarity and to insure that there is proper antecedent basis throughout the claims.

In view of the foregoing, it is respectfully submitted that claims 78 and 80-82 are not anticipated by Johnson et al..

Regarding claim 83, the Examiner asserts that Johnson et al. teaches a method for operating a receiver circuit as claimed. Specifically, the Examiner asserts that Johnson et al. teaches passing data through the receive end (FIG. 2, SRAM to 61 to 49 to 47 to DQ) in a normal operating mode, and to provide for generation of a receive repeating pattern (FIG. 8, 107) when in test mode (FIG. 8 connected to DQ).

However, it is respectfully submitted that the Examiner has failed to address several recited features of claim 83. For instance, claim 83 recites passing receive data through the receive circuit when the receive circuit is operating in a normal mode. Contrary to the assertions of the Examiner, it is respectfully submitted that Figure 2 of Johnson et al., and the path from SRAM to 61 to 49 to 47 to DQ in Figure 2 in particular, shows data being transmitted from an SLDRAM module 11 (see column 4, lines 15-46). The data is in fact transmitted from the SLDRAM module 11 and received at a memory controller 13. Thus, Applicants respectfully request that the Examiner

specifically address what elements of Johnson et al., if any, perform the claimed function of passing receive data through the receive circuit when the receive circuit is operating in a normal mode, as claimed.

Claim 83 also recites generating a receive repeating pattern in the receive circuit when the receive circuit is operating in a test mode. Since the memory controller 13 is actually acting as a receive circuit in accordance with the reasoning set forth by the Examiner, it is respectfully submitted that Johnson et al. does not teach that a receive repeating pattern is generated in the SLDRAM module 11. The Examiner acknowledges this by asserting that a synchronizing pattern may be generated in the circuit of Figure 8, which is located in the control logic circuit 21 of the SLDRAM module 11 of Figure 2 (see column 5, lines 59-62). Also, the Examiner incorrectly asserts that the circuit of Figure 8 (i.e., the control logic circuit 21 of the SLDRAM module 11 of Figure 2) is connected to the DQ bus in Figure 2. Figure 2 clearly shows that this assertion is incorrect. Thus, Applicants respectfully request that the Examiner specifically address what elements of Johnson et al., if any, perform the claimed function of generating a receive repeating pattern in the receive circuit when the receive circuit is operating in a test mode, as

claimed.

Lastly, claim 83 is directed toward a method for operating a receive circuit to provide for evaluation of a digital signaling system. In contrast, Johnson et al. is directed (as acknowledged by the Examiner) toward a method of calibrating a data path. It is respectfully submitted that evaluating is different than calibrating, as the former does not necessarily include the latter.

In view of the foregoing, it is respectfully submitted that claim 83 is not anticipated by Johnson et al..

Claims 84-88 are dependent upon independent claim 83. Thus, since independent claim 83 should be allowable as discussed above, claims 84-88 should also be allowable at least by virtue of their dependency on independent claim 83. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 84 recites that the step of generating a receive repeating pattern in the receive circuit further comprises the step of preloading an initialization pattern into the receive circuit. It is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature. Also, claim 85 recites that the step of generating a receive repeating pattern

in the receive circuit further comprises the step of uniting a plurality of pipeline structures within the receive circuit into a receive repeating pattern generator when the receive circuit is operating in the test mode. As previously discussed in the Amendment/Response filed May 17, 2004, it is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature. Further, claim 86 recites that the step of passing receive data through the receive circuit further comprises the step of passing distinct data through each of the plurality of pipeline structures when the receive circuit is operating in the normal mode. As previously discussed in the Amendment/Response filed May 17, 2004, it is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature. Additionally, claim 87 recites that the method further comprises the steps of transmitting the receive data to the receive circuit from a transmit circuit when the receive circuit is operating in the normal mode, and transmitting a transmit repeating pattern to the receive circuit from the transmit circuit when the receive circuit is operating in the test mode. It is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature. Moreover, claim 88 recites that the method further comprises the steps of transmitting the receive data to the receive circuit

from a transmit circuit when the receive circuit is operating in the normal mode, and transmitting a transmit repeating pattern to the receive circuit from a test transmitter separate from the transmit circuit when the receive circuit is operating in the test mode. It is respectfully submitted that Johnson et al. fails to claim, disclose, or even suggest such a feature.

At this point it should be noted that claims 86-88 have been amended solely for purposes of clarity and to insure that there is proper antecedent basis throughout the claims.

In view of the foregoing, it is respectfully submitted that claims 84-88 are not anticipated by Johnson et al..

Accordingly, it is respectfully requested that the aforementioned anticipation rejection of claims 77, 78, and 80-88 be withdrawn.

IV. THE OBVIOUSNESS REJECTION OF CLAIMS 1, 3, 4, 9, 10, 41 & 46

Claims 1, 3, 4, 9, 10, 41, and 46 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847). This rejection is hereby respectfully traversed.

As stated in MPEP § 2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references

themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Also, as stated in MPEP § 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Further, as stated in MPEP § 2143.01, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re

Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). That is, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970). Additionally, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). Finally, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Regarding claim 1, the Examiner asserts that Gauthier et al. teaches a method of testing a circuit by first generating a repeating transmission pattern, transmitting the pattern to a receiver, generating a receive pattern, and comparing the two patterns (see column 5 lines 23-43). The Examiner acknowledges that Gauthier et al. does not teach the adjustment of a parameter that affects reception of the repeating pattern. However, the Examiner then asserts that Chao et al. does teach this limitation (see Abstract and column 6 lines 11-55). The Examiner goes on to assert that one with ordinary skill in the art at the time of the invention, motivated by Chao et al.,

would find it obvious to combine Gauthier et al. and Chao et al. so as to arrive at the claimed invention.

However, it is respectfully submitted that the Examiner has failed to address several recited features of claim 1. For instance, claim 1 recites generating a transmit repeating pattern in a transmit circuit, transmitting the transmit repeating pattern to a receive circuit, generating a receive repeating pattern in the receive circuit, and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison. In contrast, it is respectfully submitted that Gauthier et al. does not teach a transmit circuit that generates a transmit pattern and then transmits the transmit pattern to a receive circuit, which generates a receive pattern for comparison with the transmit pattern. That is, it is respectfully submitted that Gauthier et al. merely shows a first LFSR 5 which generates a first pattern that is transmitted to a circuit under test 20 (see column 3, lines 5-24). This circuit under test 20 does not generate a second pattern. Rather, the second pattern is generated by a second LFSR 50 (see column 3, lines 36-37). Granted, the second LFSR 50 does receive an LSB portion of one word of a "tested" pattern from the circuit under test 20 once during an initialization process (see column 4, lines 44-48). However, this single occurrence of the LSB

portion of one word of the "tested" pattern from the circuit under test 20 is certainly not the first pattern from the first LFSR 5.

It is also respectfully submitted that it would not have been obvious to combine Gauthier et al. and Chao et al., and even if they were combined the result would not be the claimed invention. For instance, Gauthier et al. teaches a pass/fail method of testing transmission paths, while Chao et al. teaches a clock varying method of testing I/O circuits. Since Gauthier et al. does not disclose any need for adjusting any parameters in its test method, and Chao et al. does not disclose any need for generating two sets of patterns, there would not have been any reason or motivation to combine Gauthier et al. and Chao et al..

Furthermore, even if Gauthier et al. and Chao et al. were combined, no benefit would be realized from the combination of these two disparate circuits. Indeed, by modifying the test circuit of Gauthier et al. with varying clock signals of Chao et al., one would merely arrive at a pass/fail method of testing transmission paths wherein both first and second patterns are generated with varying clock signals, which would not result in any benefit and indeed may make the method inoperable.

In view of the foregoing, it is respectfully submitted that claim 1 is not obvious in view of Gauthier et al. and Chao et al..

Claims 3, 4, 9, 10, 41, and 46 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 3, 4, 9, 10, 41, and 46 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 1, 3, 4, 9, 10, 41, and 46 be withdrawn.

V. THE OBVIOUSNESS REJECTION OF CLAIM 2

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Whitworth et al. (U.S. Patent No. 6,331,787). This rejection is hereby respectfully traversed.

Claim 2 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above,

claim 2 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 2 be withdrawn.

VI. THE OBVIOUSNESS REJECTION OF CLAIMS 5, 14-16, 18 & 19

Claims 5, 14-16 18, and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Foland, Jr. et al. (U.S. Patent No. 5,761,212). This rejection is hereby respectfully traversed.

Claims 5, 14-16 18, and 19 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 5, 14-16 18, and 19 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 5, 14-16 18, and 19 be withdrawn.

VII. THE OBVIOUSNESS REJECTION OF CLAIM 17

Claim 17 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) in view of Foland, Jr. et al. (U.S. Patent No. 5,761,212) and further in view of Couch (U.S. Patent No. 4,475,210). This rejection is hereby respectfully traversed.

Claim 17 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 17 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 17 be withdrawn.

VIII. THE OBVIOUSNESS REJECTION OF CLAIM 6

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Sakoda et al. (U.S. Patent No. 6,230,022). This rejection is hereby respectfully traversed.

Claim 6 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 6 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 6 be withdrawn.

IX. THE OBVIOUSNESS REJECTION OF CLAIM 7

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Terry (U.S. Patent No. 6,055,297). This rejection is hereby respectfully traversed.

Claim 7 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 7 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 7 be withdrawn.

X. THE OBVIOUSNESS REJECTION OF CLAIM 8

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Liau et al. (U.S. Patent No. 6,650,698). This rejection is hereby respectfully traversed.

Claim 8 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 8 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even

suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 8 be withdrawn.

XI. THE OBVIOUSNESS REJECTION OF CLAIMS 11, 31-35, & 38

Claims 11, 31-35, and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Maddux et al. (U.S. Patent No. 6,421,801). This rejection is hereby respectfully traversed.

Claims 11, 31-35, and 38 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 11, 31-35, and 38 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 11, 31-35, and 38 be withdrawn.

XII. THE OBVIOUSNESS REJECTION OF CLAIM 12

Claim 12 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Prentice (U.S. Patent No. 6,674,998). This rejection is hereby respectfully traversed.

Claim 12 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 12 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 12 be withdrawn.

XIII. THE OBVIOUSNESS REJECTION OF CLAIM 13

Claim 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Berkovich (U.S. Patent No. 5,369,755). This rejection is hereby respectfully traversed.

Claim 13 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 13 should also be allowable at least by virtue of its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 13 be withdrawn.

XIV. THE OBVIOUSNESS REJECTION OF CLAIMS 20-22 & 24-30

Claims 20-22 and 24-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) in view of Foland, Jr. et al. (U.S. Patent No. 5,761,212) and further in view of Johnson et al. (U.S. Patent

No. 6,606,041). This rejection is hereby respectfully traversed.

Claims 20-22 and 24-30 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 20-22 and 24-30 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 20-22 and 24-30 be withdrawn.

XV. THE OBVIOUSNESS REJECTION OF CLAIM 23

Claim 23 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) in view of Foland, Jr. et al. (U.S. Patent No. 5,761,212) and further in view of Komatsu et al. (U.S. Patent No. 6,631,486). This rejection is hereby respectfully traversed.

Claim 23 is dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claim 23 should also be allowable at least by virtue of

its dependency on independent claim 1. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 23 be withdrawn.

XVI. THE OBVIOUSNESS REJECTION OF CLAIMS 36 & 37

Claims 36 and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Maddux et al. (U.S. Patent No. 6,421,801) and further in view of Johnson et al. (U.S. Patent No. 6,606,041). This rejection is hereby respectfully traversed.

Claims 36 and 37 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 36 and 37 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 36 and 37 be withdrawn.

XVII. THE OBVIOUSNESS REJECTION OF CLAIMS 39 & 40

Claims 39 and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) in view of Foland, Jr. et al. (U.S. Patent No. 5,761,212) and further in view of Sakoda et al. (U.S. Patent No. 6,230,022). This rejection is hereby respectfully traversed.

Claims 39 and 40 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 39 and 40 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 39 and 40 be withdrawn.

XVIII. THE OBVIOUSNESS REJECTION OF CLAIMS 42 & 43

Claims 42 and 43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Johnson et al. (U.S. Patent No. 6,606,041). This rejection is hereby respectfully traversed.

Claims 42 and 43 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 42 and 43 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 42 and 43 be withdrawn.

XIX. THE OBVIOUSNESS REJECTION OF CLAIMS 44, 45, 47, & 48

Claims 44, 45, 47, and 48 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) in view of Chao et al. (U.S. Patent No. 6,671,847) and further in view of Jalali et al. (U.S. Patent No. 6,154,659). This rejection is hereby respectfully traversed.

Claims 44, 45, 47, and 48 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 44, 45, 47, and 48 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 44, 45, 47, and 48 be withdrawn.

XX. THE OBVIOUSNESS REJECTION OF CLAIMS 49-53 & 56

Claims 49-53 and 56 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gerowitz et al. (U.S. Patent No. 6,222,380) in view of Gauthier et al. (U.S. Patent No. 5,228,042). This rejection is hereby respectfully traversed.

Regarding claim 49, the Examiner asserts that Gerowitz et al. teaches a transmit data storage element (FIG. 2, L1, L2, L3, L4) adapted to receive data from a transmit data input (FIG. 2, DO, D1, D2, D3) to be sequentially transmitted as transmit data out when operating in normal mode (FIG. 2, Q). The Examiner acknowledges that Gerowitz et al. does not teach a repeating pattern in a test mode. However, the Examiner then asserts that

Gauthier et al. does teach providing a repeating pattern (FIG. 1, 5) in a test mode (FIG. 1, Control Circuit 30) and transmitting the data out. The Examiner goes on to assert that by joining the multiplexers of the two references (Gauthier et al., FIG. 1, 15 and Gerowitz et al., FIG. 2, 21), one would have a data storage element consisting of both latches (in Gerowitz et al.), and a shift register (in Gauthier et al.), and one would be able to provide a sequentially transmitted repeating pattern in test mode, or normal data when not in test mode. The Examiner also goes on to assert that Gauthier et al. (in column 1, lines 43-52) states as an advantage an improved method and circuit for test, utilizing less test hardware memory. The Examiner further goes on to assert that one with ordinary skill in the art at the time of the invention, motivated as indicated by Gauthier et al., would find it obvious to combine Gerowitz et al. and Gauthier et al. so as to arrive at the claimed invention.

However, it is respectfully submitted that Gerowitz et al. does not teach a transmit data storage element configured to receive data from a transmit data input and sequentially transmit a transmit data output signal when the transmit circuit is operating in a normal mode, as presently claimed. That is, the latches (L1, L2, L3, & L4) in Figure 2 of Gerowitz et al. do

not both receive data from a transmit data input and sequentially transmit a transmit data output signal. Rather, the latches (L1, L2, L3, & L4) in Figure 2 of Gerowitz et al. merely latch parallel data, and then output this same parallel data. It is respectfully submitted that this latching and subsequent outputting of parallel data does not teach sequentially transmit a transmit data output signal, as claimed.

Also, it is respectfully submitted that it would not have been obvious to combine Gerowitz et al. and Gauthier et al., and even if they were combined the result would not be the claimed invention. For instance, Gerowitz et al. teaches a high speed parallel/serial link for data communication, which does not include or even suggest a mode or mechanism for testing the link. In contrast, Gauthier et al. teaches a pass/fail method of testing transmission paths, wherein data is not converted from parallel to serial, or vice versa. Since Gerowitz et al. does not disclose any need or interest in testing its link, but rather is mainly interested in parallel to serial conversion and reducing pin count, and Gauthier et al. is only interested in transmission path testing, with no parallel to serial conversion and no apparent regard for pin count, it is respectfully submitted that there would not have been any reason or motivation to combine Gerowitz et al. and Gauthier et al..

Furthermore, even if Gerowitz et al. and Gauthier et al. were combined, no benefit would be realized from the combination of these two disparate circuits. For instance, the Examiner asserts that combining the multiplexer 21 in Gerowitz et al. with the multiplexer 15 in Gauthier et al. would result in a data storage element having both latches (in Gerowitz et al.) and a shift register (in Gauthier et al.) for providing a sequentially transmitted repeating pattern in test mode, or normal data when not in test mode. However, Applicants respectfully disagree for several reasons. First of all, claim 49 recites that a transmit data storage element (i.e., not two transmit data storage elements formed from latches in Gerowitz et al. and a shift register in Gauthier et al.) is operative in both a normal mode and a test mode. Secondly, as discussed above, the latches in Gerowitz et al. do not sequentially transmit a transmit data output signal. Thirdly, the multiplexer 21 in Gerowitz et al. differs from the multiplexer 15 in Gauthier et al. in that the multiplexer 21 in Gerowitz et al. operates to multiplex parallel input data into serial output data while the multiplexer 15 in Gauthier et al. operates to select between test data and normal data, with no parallel to serial conversion. Thus, the combination of the multiplexer 21 in Gerowitz et al. and the multiplexer 15 in Gauthier et al.

would not result in any benefit and indeed may make a resulting circuit inoperable.

At this point it should be noted that claim 49 has been amended solely for purposes of complying with the Examiner's request to replace the term "adapted" with some other positive recitation (see Examiner's objection to claims 90-93).

In view of the foregoing, it is respectfully submitted that claim 49 is not obvious in view of Gerowitz et al. and Gauthier et al..

Claims 50-53 and 56 are dependent upon independent claim 49. Thus, since independent claim 49 should be allowable as discussed above, claims 50-53 and 56 should also be allowable at least by virtue of their dependency on independent claim 49. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 49-53 and 56 be withdrawn.

XXI. THE OBVIOUSNESS REJECTION OF CLAIM 57

Claim 57 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gerowitz et al. (U.S. Patent No. 6,222,380) in

view of Gauthier et al. (U.S. Patent No. 5,228,042) and further in view of applicant's admitted prior art. This rejection is hereby respectfully traversed.

Claim 57 is dependent upon independent claim 49. Thus, since independent claim 49 should be allowable as discussed above, claim 57 should also be allowable at least by virtue of its dependency on independent claim 49. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 57 be withdrawn.

XXII. THE OBVIOUSNESS REJECTION OF CLAIM 58

Claim 58 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gerowitz et al. (U.S. Patent No. 6,222,380) in view of Gauthier et al. (U.S. Patent No. 5,228,042) and further in view of Jalali et al. (U.S. Patent No. 6,154,659). This rejection is hereby respectfully traversed.

Claim 58 is dependent upon independent claim 49. Thus, since independent claim 49 should be allowable as discussed above, claim 58 should also be allowable at least by virtue of

its dependency on independent claim 49. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 58 be withdrawn.

XXIII. THE OBVIOUSNESS REJECTION OF CLAIM 59

Claim 59 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gerowitz et al. (U.S. Patent No. 6,222,380) in view of Gauthier et al. (U.S. Patent No. 5,228,042) in view of Jalali et al. (U.S. Patent No. 6,154,659) and further in view of Johnson et al. (U.S. Patent No. 6,606,041). This rejection is hereby respectfully traversed.

Claim 59 is dependent upon independent claim 49. Thus, since independent claim 49 should be allowable as discussed above, claim 59 should also be allowable at least by virtue of its dependency on independent claim 49. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 59 be withdrawn.

XXIV. THE OBVIOUSNESS REJECTION OF CLAIM 60

Claim 60 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gerowitz et al. (U.S. Patent No. 6,222,380) in view of Gauthier et al. (U.S. Patent No. 5,228,042) in view of Jalali et al. (U.S. Patent No. 6,154,659) in view of Johnson et al. (U.S. Patent No. 6,606,041) and further in view of Chen (U.S. Patent No. 6,003,118). This rejection is hereby respectfully traversed.

Claim 60 is dependent upon independent claim 49. Thus, since independent claim 49 should be allowable as discussed above, claim 60 should also be allowable at least by virtue of its dependency on independent claim 49. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 60 be withdrawn.

XXV. THE OBVIOUSNESS REJECTION OF CLAIMS 61-65, 68, & 70

Claims 61-65, 68, and 70 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga (U.S. Patent No. 6,339,387) in view of Gauthier et al. (U.S. Patent No. 5,228,042). This rejection is hereby respectfully traversed.

Regarding claim 61, the Examiner asserts that Koga teaches a receive data storage element (FIG. 1, C8, C9, C10, C7) adapted to output data from a receive data input (FIG. 1, DATA) when operating in normal mode. The Examiner acknowledges that Koga does not teach a comparison element in a test mode. However, the Examiner then asserts that Gauthier et al. does teach providing a comparison element (FIG. 1, 60) in a test mode (FIG. 1, Control Circuit 30), comparing the received with the expected producing an output signal (FIG. 1, 62). The Examiner goes on to assert that by joining the two references (Gauthier et al., FIG. 1, 21 and Koga, FIG. 1, DATA), one would have a data storage element consisting of both latches (in Koga) and a shift register (in Gauthier et al.), and one would be able to evaluate a transmitted repeating pattern in test mode, or normal data when not in test mode. The Examiner also goes on to assert that Gauthier et al. (in column 1, lines 43-52) states as an advantage an improved method and circuit for test, utilizing less test hardware memory. The Examiner further goes on to

assert that one with ordinary skill in the art at the time of the invention, motivated as indicated by Gauthier et al., would find it obvious to combine Koga and Gauthier et al. so as to arrive at the claimed invention.

However, it is respectfully submitted that it would not have been obvious to combine Koga and Gauthier et al., and even if they were combined the result would not be the claimed invention. For instance, Koga teaches a serial to parallel converter, but does not include or even suggest a mode or mechanism for testing the conversion. In contrast, Gauthier et al. teaches a pass/fail method of testing transmission paths, wherein data is not converted from serial to parallel, or vice versa. Since Koga is only interested in serial to parallel conversion and does not disclose any need or interest in the testing of same, and Gauthier et al. is only interested in transmission path testing, with no serial to parallel conversion, it is respectfully submitted that there would not have been any reason or motivation to combine Koga and Gauthier et al..

Furthermore, even if Koga and Gauthier et al. were combined, no benefit would be realized from the combination of these two disparate circuits. For instance, the Examiner asserts that combining Koga with Gauthier et al. would result in

a data storage element having both latches (in Koga) and a shift register (in Gauthier et al.) for evaluating a transmitted repeating pattern in test mode, or normal data when not in test mode. However, Applicants respectfully disagree for multiple reasons. First of all, claim 61 recites that a receive data storage element (i.e., not two receive data storage elements formed from latches in Koga and a shift register in Gauthier et al.) is operative in both a normal mode and a test mode. Secondly, as discussed above, Koga is directed toward serial to parallel conversion, while Gauthier et al. does not teach or even suggest such a conversion. Thus, the combination of Koga and Gauthier et al. would not result in any benefit and indeed may make a resulting circuit inoperable.

At this point it should be noted that claim 61 has been amended solely for purposes of complying with the Examiner's request to replace the term "adapted" with some other positive recitation (see Examiner's objection to claims 90-93).

In view of the foregoing, it is respectfully submitted that claim 61 is not obvious in view of Koga and Gauthier et al..

Claims 62-65, 68, and 70 are dependent upon independent claim 61. Thus, since independent claim 61 should be allowable as discussed above, claims 62-65, 68, and 70 should also be allowable at least by virtue of their dependency on independent

claim 61. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 61-65, 68, and 70 be withdrawn.

XXVI. THE OBVIOUSNESS REJECTION OF CLAIM 69

Claim 69 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga (U.S. Patent No. 6,339,387) in view of Gauthier et al. (U.S. Patent No. 5,228,042) and further in view of Johnson et al. (U.S. Patent No. 6,606,041). This rejection is hereby respectfully traversed.

Claim 69 is dependent upon independent claim 61. Thus, since independent claim 61 should be allowable as discussed above, claim 69 should also be allowable at least by virtue of its dependency on independent claim 61. Moreover, this claim recites additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 69 be withdrawn.

XXVII. THE OBVIOUSNESS REJECTION OF CLAIMS 71-74

Claims 71-74 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga (U.S. Patent No. 6,339,387) in view of Gauthier et al. (U.S. Patent No. 5,228,042) and further in view of Maddux et al. (U.S. Patent No. 6,421,801). This rejection is hereby respectfully traversed.

Claims 71-74 are dependent upon independent claim 61. Thus, since independent claim 61 should be allowable as discussed above, claims 71-74 should also be allowable at least by virtue of their dependency on independent claim 61. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 71-74 be withdrawn.

XXVIII. THE OBVIOUSNESS REJECTION OF CLAIM 89

Claim 89 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gauthier et al. (U.S. Patent No. 5,228,042) and further in view of Chao et al. (U.S. Patent No. 6,421,801). This rejection is hereby respectfully traversed.

Claim 89 is somewhat similar in scope to claim 1. Accordingly, for the reasons set forth above with respect to claim 1, it is respectfully submitted that claim 89 is not obvious in view of Gauthier et al. and Chao et al..

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 89 be withdrawn.

XXIX. THE OBVIOUSNESS REJECTION OF CLAIM 90

Claim 90 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gerowitz et al. (U.S. Patent No. 6,222,380) in view of Gauthier et al. (U.S. Patent No. 5,228,042). This rejection is hereby respectfully traversed.

Claim 90 is somewhat similar in scope to claim 49. Accordingly, for the reasons set forth above with respect to claim 49, it is respectfully submitted that claim 90 is not obvious in view of Gerowitz et al. and Gauthier et al..

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 90 be withdrawn.

XXX. THE OBVIOUSNESS REJECTION OF CLAIM 91

Claim 91 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Pyhalammi (U.S. Patent No. 5,273,561) in view of Gauthier et al. (U.S. Patent No. 5,228,042). This rejection is hereby respectfully traversed.

As acknowledged by the Examiner, Pyhalammi fails teach anything regarding different modes, particularly a test mode. Also, Gauthier et al. fails to teach receiving and transmitting different serial data depending upon mode. Thus, there would have been no motivation to combine Pyhalammi and Gauthier et al. so as to arrive at the claimed invention. Additionally, even if Pyhalammi and Gauthier et al. were combined, the resulting combination would not resemble the claimed invention, but rather a system always operating in a single mode (i.e., either normal or test). Accordingly, it is respectfully submitted that claim 91 is not obvious in view of Pyhalammi and Gauthier et al..

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 91 be withdrawn.

XXXI. THE OBVIOUSNESS REJECTION OF CLAIM 92

Claim 92 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Koga (U.S. Patent No. 6,339,387) in view of

Gauthier et al. (U.S. Patent No. 5,228,042). This rejection is hereby respectfully traversed.

Claim 92 is somewhat similar in scope to claim 61. Accordingly, for the reasons set forth above with respect to claim 61, it is respectfully submitted that claim 92 is not obvious in view of Koga and Gauthier et al..

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 92 be withdrawn.

XXXII. THE OBVIOUSNESS REJECTION OF CLAIM 93

Claim 93 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Pyhalammi (U.S. Patent No. 5,273,561) in view of Gauthier et al. (U.S. Patent No. 5,228,042). This rejection is hereby respectfully traversed.

Claim 93 is somewhat similar in scope to claims 61 and 91. Accordingly, for the reasons set forth above with respect to claims 61 and 91, it is respectfully submitted that claim 93 is not obvious in view of Pyhalammi and Gauthier et al..

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claim 93 be withdrawn.

XXXIII. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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Date: May 9, 2005

APPENDIX A

1 (original). A method for evaluating a digital signaling system comprising the steps of:

generating a transmit repeating pattern in a transmit circuit;

transmitting the transmit repeating pattern to a receive circuit;

generating a receive repeating pattern in the receive circuit;

comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison; and

adjusting a parameter affecting reception of the transmit repeating pattern at the receive circuit.

2 (original). The method of claim 1 wherein the parameter is a termination setting.

3 (original). The method of claim 1 wherein the parameter is a transmit clock offset.

4 (original). The method of claim 1 wherein the parameter is a receive clock offset.

5 (original). The method of claim 1 wherein the parameter is an input receiver window.

6 (original). The method of claim 1 wherein the parameter is an output drive level.

7 (original). The method of claim 1 wherein the parameter is a crosstalk cancellation coefficient.

8 (original). The method of claim 1 wherein the parameter is an equalization coefficient.

9 (original). The method of claim 1 wherein the step of generating a transmit repeating pattern in a transmit circuit comprises the step of:

utilizing a shift register to generate the transmit repeating pattern.

10 (original). The method of claim 9 wherein the step of utilizing a shift register to generate the transmit repeating pattern comprises the step of:

utilizing a linear feedback shift register to generate the transmit repeating pattern.

11 (original). The method of claim 1 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a signal referenced to a ground.

12 (original). The method of claim 1 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a differential signal over a pair of conductors.

13 (original). The method of claim 1 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously.

14 (original). The method of claim 1 further comprising the step of:

setting the parameter affecting reception of the transmit repeating pattern at the receive circuit.

15 (original). The method of claim 1 wherein the step of adjusting the parameter affecting reception of the transmit repeating pattern at the receive circuit is repeated over a range of values of the parameter.

16 (original). The method of claim 15 wherein the steps of transmitting the transmit repeating pattern to the receive circuit and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison are repeated after the step of adjusting the parameter affecting reception of the transmit repeating pattern at the receive circuit is performed.

17 (original). The method of claim 16 further comprising the step of:

constructing a representation of a waveform based on the comparison.

18 (original). The method of claim 1 further comprising the step of:

selecting a value of the parameter so as to optimize reception at the receive circuit of a transmit data output

signal transmitted by the transmit circuit.

19 (original). The method of claim 18 wherein the transmit repeating pattern and the transmit data output signal are communicated from the transmit circuit to the receive circuit over a common medium.

20 (original). The method of claim 19 wherein the common medium is a data line.

21 (original). The method of claim 19 wherein the common medium is an address line.

22 (original). The method of claim 19 wherein the common medium is a control line.

23 (previously presented). The method of claim 18 wherein at least one medium is used to communicate the transmit data output signal but not to communicate the transmit repeating pattern.

24 (original). The method of claim 23 wherein the at least one medium is a data line.

25 (original). The method of claim 23 wherein the at least one medium is an address line.

26 (original). The method of claim 23 wherein the at least one medium is a control line.

27 (original). The method of claim 23 wherein at least one analysis medium is used to communicate the transmit repeating pattern.

28 (original). The method of claim 27 wherein the at least one analysis medium is a data line.

29 (original). The method of claim 27 wherein the at least one analysis medium is an address line.

30 (original). The method of claim 27 wherein the at least one analysis medium is a control line.

31 (original). The method of claim 1 wherein the receive repeating pattern is repeated with a first period and the transmit repeating pattern is repeated with a second period, the first period and the second period bearing a multiple and

submultiple relationship to each other.

32 (original). The method of claim 31 wherein the first period and the second period are equal.

33 (original). The method of claim 31 wherein the step of comparing the transmit repeating pattern and the receive repeating pattern is performed over multiple instances of the first period and the second period.

34 (original). The method of claim 33 wherein the step of adjusting the parameter occurs in the transmit circuit.

35 (original). The method of claim 33 wherein the step of adjusting the parameter occurs in the receive circuit.

36 (original). The method of claim 35 wherein the parameter affects reception of a receive data input signal, the receive data input signal communicated along a first medium used to transmit the transmit repeating pattern to the receive circuit.

37 (original). The method of claim 36 wherein the parameter further affects reception of a second receive data input signal,

the second receive data input signal communicated along a second medium, the second medium being distinct from the first medium.

38 (original). The method of claim 1 wherein the step of generating the transmit repeating pattern is performed so that the transmit repeating pattern is clocked at a transmit clock rate and the step of generating the receive repeating pattern is performed so that the receive repeating pattern is clocked at a receive clock rate, the transmit clock rate and the receive clock rate bearing a multiple and submultiple relationship to each other.

39 (original). The method of claim 1 further comprising the step of:

adjusting a second parameter affecting reception of the transmit repeating pattern at the receive circuit.

40 (original). The method of claim 39 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern comprises the step of:

comparing over a first range of the parameter and a second range of the second parameter.

41 (original). The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern comprises the step of:

detecting non-repeatability in a relationship between the transmit repeating pattern and the receive repeating pattern.

42 (original). The method of claim 41 wherein the step of adjusting the parameter further comprises the step of:

adjusting the parameter based on the non-repeatability.

43 (original). The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison is performed at system start-up.

44 (original). The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison is performed upon detection of a communication failure.

45 (original). The method of claim 1 wherein the step of comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison is performed

occasionally between periods of communication of user data between the transmit circuit and the receive circuit.

46 (original). The method of claim 1 wherein the transmit circuit and the receive circuit are located within the digital signaling system being evaluated.

47 (original). The method of claim 1 wherein the transmit circuit is located external to the digital signaling system being evaluated.

48 (original). The method of claim 1 wherein the receive circuit is located external to the digital signaling system being evaluated.

49 (previously presented). A transmit circuit comprising:

a transmit data storage element ~~adapted~~ configured to receive data from a transmit data input and sequentially transmit a transmit data output signal when the transmit circuit is operating in a normal mode, the transmit data storage element further ~~adapted~~ configured to provide a repeating pattern signal when the transmit circuit is operating in a test mode, the transmit circuit sequentially transmitting the transmit data

output signal based on the repeating pattern signal when the transmit circuit is operating in the test mode.

50 (original). The transmit circuit of claim 49 wherein the transmit data storage element comprises a shift register.

51 (original). The transmit circuit of claim 49 further comprising:

a test loop coupled to the transmit data storage element when the transmit circuit is operating in the test mode, the test loop providing feedback to allow the transmit data storage element to provide the repeating pattern signal.

52 (original). The transmit circuit of claim 49 wherein the repeating pattern signal has a data length greater than a data capacity of the transmit data storage element.

53 (original). The transmit circuit of claim 49 wherein the repeating pattern signal represents a sequence of data bits, the transmit data storage element storing each of the data bits.

54 (original). The transmit circuit of claim 49 wherein, when the transmit data storage element is divided into transmit data

storage sub-elements during operation in the normal mode, the transmit data storage sub-elements are combined as the transmit data storage element for providing the repeating pattern signal when the transmit circuit is operating in the test mode.

55 (original). The transmit circuit of claim 49 wherein the transmit data storage element is loaded from the transmit data input to initialize the test mode.

56 (original). The transmit circuit of claim 49 wherein the transmit data storage element is loaded from a source other than the transmit data input to initialize the test mode.

57 (original). The transmit circuit of claim 49 wherein the transmit data storage element is loaded via a parallel transmit load input.

58 (original). The transmit circuit of claim 49 wherein the transmit circuit receives an adjustment signal from a receiver circuit, the receive circuit receiving the transmit data output signal, the transmit circuit adjusting a parameter of the transmit data output signal based on the adjustment signal.

59 (original). The transmit circuit of claim 58 wherein the receive circuit is embodied in a first memory device and a second receive circuit is embodied in a second memory device.

60 (original). The transmit circuit of claim 59 wherein the transmit circuit adjusts the parameter to a first value for communication with the first memory device and to a second value for communication with the second memory device.

61 (original). A receive circuit comprising:

a receive data storage element ~~adapted~~ configured to output a receive data output signal based on a receive data input signal received at a receive data input when the receive circuit is operating in a normal mode, the receive data storage element further ~~adapted~~ configured to provide a repeating pattern signal when the receive circuit is operating in a test mode, and;

a comparison element, the comparison element ~~adapted~~ configured to perform a comparison of a relationship between the repeating pattern signal and the receive data input signal received at the receive data input and to produce a comparison output signal based on the comparison when the receive circuit is operating in the test mode.

62 (original). The receive circuit of claim 61 wherein the receive data storage element comprises a shift register.

63 (original). The receive circuit of claim 61 further comprising:

a test loop coupled to the receive data storage element when the receive circuit is operating in the test mode, the test loop providing feedback to allow the receive data storage element to provide the repeating pattern signal.

64 (original). The receive circuit of claim 61 wherein the repeating pattern signal has a data length greater than a data capacity of the receive data storage element.

65 (original). The receive circuit of claim 61 wherein the repeating pattern signal represents a sequence of data bits, the receive data storage element storing each of the data bits.

66 (original). The receive circuit of claim 61 wherein, when the receive data storage element is divided into receive data storage sub-elements during operation in the normal mode, the receive data storage sub-elements are combined as the receive data storage element for providing the repeating pattern signal

when the receive circuit is operating in the test mode.

67 (original). The receive circuit of claim 61 wherein the receive data storage element is loaded from the receive data input to initialize the test mode.

68 (original). The receive circuit of claim 61 wherein the receive data storage element is loaded from a source other than the receive data input to initialize the test mode.

69 (original). The receive circuit of claim 61 wherein the receive data storage element is loaded via a parallel receive load input

70 (original). The receive circuit of claim 61 wherein the comparison element detects variation of the relationship between the repeating pattern signal and the receive data input signal received at the receive data input.

71 (original). The receive circuit of claim 70 wherein the repeating pattern signal is repeated with a first period and the receive data input signal is repeated with a second period, the first period and the second period bearing a multiple and

submultiple relationship to each other.

72 (original). The receive circuit of claim 71 wherein the first period and the second period are equal.

73 (original). The receive circuit of claim 71 wherein the comparison of the relationship between the repeating pattern signal and the receive data input signal is performed over multiple instances of the first period and the second period.

74 (original). The receive circuit of claim 73 wherein the receive circuit communicates the comparison output signal to a source of the receive data input signal.

75 (original). The receive circuit of claim 73 wherein the receive circuit adjusts a parameter affecting its reception of the receive data input signal based on the comparison output signal.

76 (original). The receive circuit of claim 75 wherein the parameter affects reception of a second receive data input signal, the second receive data input signal being distinct from the receive data input signal.

77 (currently amended). A method for operating a transmit circuit to provide for evaluation of a digital signaling system comprising the steps of:

passing transmit data ~~to be transmitted~~ through the transmit circuit when the transmit circuit is operating in a normal mode; and

generating a transmit repeating pattern in the transmit circuit when the transmit circuit is operating in a test mode.

78 (original). The method of claim 77 wherein the step of generating a transmit repeating pattern in the transmit circuit further comprises the step of:

preloading an initialization pattern into the transmit circuit.

79 (original). The method of claim 77 wherein the step of generating a transmit repeating pattern in the transmit circuit further comprises the step of:

uniting a plurality of pipeline structures within the transmit circuit into a transmit repeating pattern generator when the transmit circuit is operating in the test mode.

80 (currently amended). The method of claim 79 wherein the step of passing transmit data ~~to be transmitted~~ through the transmit circuit further comprises the step of:

passing distinct data through each of the plurality of pipeline structures when the transmit circuit is operating in the normal mode.

81 (currently amended). The method of claim 77 further comprising the steps of:

receiving the transmit data in a receive circuit when the transmit circuit is operating in the normal mode; and

receiving the transmit repeating pattern in the receive circuit when the transmit circuit is operating in the test mode.

82 (currently amended). The method of claim 77 further comprising the steps of:

receiving the transmit data in a receive circuit when the transmit circuit is operating in the normal mode; and

receiving the transmit repeating pattern in a test receiver separate from the receive circuit when the transmit circuit is operating in the test mode.

83 (original). A method for operating a receive circuit to

provide for evaluation of a digital signaling system comprising the steps of:

passing receive data through the receive circuit when the receive circuit is operating in a normal mode; and

generating a receive repeating pattern in the receive circuit when the receive circuit is operating in a test mode.

84 (original). The method of claim 83 wherein the step of generating a receive repeating pattern in the receive circuit further comprises the step of:

preloading an initialization pattern into the receive circuit.

85 (original). The method of claim 83 wherein the step of generating a receive repeating pattern in the receive circuit further comprises the step of:

uniting a plurality of pipeline structures within the receive circuit into a receive repeating pattern generator when the receive circuit is operating in the test mode.

86 (currently amended). The method of claim 85 wherein the step of passing receive data ~~to be transmitted~~ through the receive circuit further comprises the step of:

passing distinct data through each of the plurality of pipeline structures when the receive circuit is operating in the normal mode.

87 (currently amended). The method of claim 83 further comprising the steps of:

transmitting the receive data to the receive circuit from a transmit circuit when the receive circuit is operating in the normal mode; and

transmitting a transmit repeating pattern to the receive circuit from the transmit circuit when the receive circuit is operating in the test mode.

88 (currently amended). The method of claim 83 further comprising the steps of:

transmitting the receive data to the receive circuit from a transmit circuit when the receive circuit is operating in the normal mode; and

transmitting a transmit repeating pattern to the receive circuit from a test transmitter separate from the transmit circuit when the receive circuit is operating in the test mode.

89 (previously presented). A method for improving the

operation of a digital signaling system comprising the steps of:

generating a transmit repeating pattern in a transmit circuit;

transmitting the transmit repeating pattern to a receive circuit;

generating a receive repeating pattern in the receive circuit;

comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison; and

adjusting a parameter affecting reception of the transmit repeating pattern at the receive circuit based at least in part upon the comparison.

90 (currently amended). A transmit circuit comprising:

a transmit data storage element ~~adapted~~ configured to receive parallel data from a transmit data input and sequentially transmit a serial transmit data output signal when the transmit circuit is operating in a normal mode, the transmit data storage element further ~~adapted~~ configured to provide a repeating pattern signal when the transmit circuit is operating in a test mode, the transmit circuit sequentially transmitting the serial transmit data output signal based on the repeating pattern signal when the transmit circuit is operating in the

test mode.

91 (currently amended). A transmit circuit comprising:

a transmit data storage element ~~adapted~~ configured to receive serial data from a transmit data input and sequentially transmit a serial transmit data output signal when the transmit circuit is operating in a normal mode, the transmit data storage element further ~~adapted~~ configured to provide a repeating pattern signal when the transmit circuit is operating in a test mode, the transmit circuit sequentially transmitting the serial transmit data output signal based on the repeating pattern signal when the transmit circuit is operating in the test mode.

92 (currently amended). A receive circuit comprising:

a receive data storage element ~~adapted~~ configured to output a parallel receive data output signal based on a serial receive data input signal received at a receive data input when the receive circuit is operating in a normal mode, the receive data storage element further ~~adapted~~ configured to provide a repeating pattern signal when the receive circuit is operating in a test mode, and;

a comparison element, the comparison element ~~adapted~~ configured to perform a comparison of a relationship between the

repeating pattern signal and the serial receive data input signal received at the receive data input and to produce a comparison output signal based on the comparison when the receive circuit is operating in the test mode.

93 (currently amended). A receive circuit comprising:

a receive data storage element ~~adapted~~ configured to output a serial receive data output signal based on a serial receive data input signal received at a receive data input when the receive circuit is operating in a normal mode, the receive data storage element further ~~adapted~~ configured to provide a repeating pattern signal when the receive circuit is operating in a test mode, and;

a comparison element, the comparison element ~~adapted~~ configured to perform a comparison of a relationship between the repeating pattern signal and the serial receive data input signal received at the receive data input and to produce a comparison output signal based on the comparison when the receive circuit is operating in the test mode.